In the claims:

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1. (Currently Amended) A pipelined multistreaming processor, comprising:

an instruction source;

a plurality of streams ~~fetching~~ enabled to fetch instructions at different times from the instruction source;

a dispatch stage for selecting and dispatching instructions to a set of execution units;

a set of instruction queues having one queue associated with each stream in the plurality of streams, and located in the pipeline between the instruction source and the dispatch stage; and

a select system for selecting streams in each cycle to fetch instructions from the instruction source~~;~~

~~characterized in that the number of streams selected for which to fetch instructions in each cycle is fewer than the number of streams in the plurality of streams.~~ wherein the select system selects a number of streams for which to fetch instructions, which are fewer in number than the number of streams in the plurality of streams.

2. (Original) The processor of claim 1 wherein the number of streams in the plurality of streams is eight, and the number of streams selected for which to fetch instructions in each cycle is two.

3. (Currently Amended) The processor of claim 2 wherein the select system monitors a set of fetch program counters (FPC) having one FPC associated with each stream, and directs fetching if instructions beginning at addresses according to the ~~to the~~ program counters.

4. (Currently Amended) The processor of claim 2 wherein each stream selected to fetch is directed to fetch eight instructions from the instruction ~~cache~~ source.

5. (Cancelled)

6. (Currently Amended) The processor of claim ~~5~~ 1 wherein the set of execution units comprises eight Arithmetic-Logic Units (ALUs), and two memory units.

7. (Currently Amended) In a pipelined multistreaming processor having an instruction queue, a method for ~~decoupling~~ disassociating fetching from a dispatch stage, comprising the steps of:

(a) placing a set of instruction queues, one instruction queue for each stream, in the pipeline between the instruction ~~queue~~ source and the dispatch stage; and

(b) selecting one or more streams, fewer than the number of streams in the multistreaming processor, for which to fetch instructions in each cycle from an instruction source.

8. (Original) The method of claim 7 wherein the number of streams in the plurality of streams is eight, and the number of streams selected for which to fetch instructions in each cycle is two.

9. (Currently Amended) The method of claim 8 wherein the select system monitors a set of fetch program counters (FPC) having one FPC associated with each stream, and directs fetching if instructions beginning at addresses according to the ~~to the~~ program counters.

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10. (Original) The method of claim 7 wherein each stream selected to fetch is directed to fetch eight instructions from the instruction source.

11. (Currently Amended) The method of claim ~~6~~ 7wherein the dispatch stage dispatches instructions to a set of execution units.

12. (Currently Amended) The method of claim 11 wherein the set of execution units comprises eight Arithmetic-Logic Units ~~(ALS)~~ (ALUs), and two memory ports.